REMARKS

By this amendment, claim 9 is canceled. Claims 7, 13-15, and 17 are amended. Claims 1-8 and 10-23 remain pending in the application.

Alleged Anticipation of claims 1-6 by Wu

In the Office Action, claims 1-6 were rejected under 35 U.S.C. §102(b) as allegedly being anticipated by Wu, U.S. Patent No. 5,659,715 ("Wu"). The Applicants respectfully traverse the rejection.

In the Specification, the Applicants claim priority from U.S. Provisional Application No. 60/065,855 entitled "Multipurpose Digital Signal Processing System" filed on November 14, 1997. Since Wu was issued on August 19, 1997, a priority date of November 14, 1997 renders a rejection under 35 U.S.C. §102(b) improper.

Claims 1-6 recite, *inter alia*, a first memory portion including a first number of a plurality of memory **banks** and a second memory portion including a second number of a plurality of memory **banks**.

The Office Action alleges that Wu discloses a first memory portion including a first number of a plurality of memory banks and a second memory portion including a plurality of memory banks (See Office Action, page 2, para. 3). The Applicants respectfully disagree.

Wu appears to disclose an adjustable memory map for an integrated single shared memory bank (See Wu, col. 7, lines 15-16). Wu's integrated single shared memory bank is controlled as a single block of memory (See Wu, col. 7, lines 55-58).

Wu appears to disclose an optional expansion capability (See Wu, col. 7, lines 26-27). However, this memory expansion is integrated into Wu's shared memory as an enlargement of the single block of memory (See Wu, col. 7, lines 45-48).

Wu discloses that the integrated single shared memory bank is assigned in **byte** increments (see Wu, col. 7, lines 24-35).

In contrast, claims 1-6 recite, *inter alia*, a first memory portion including a first number of a plurality of memory **banks** and a second memory portion including a second number of a plurality of memory **banks**. Hence, memory is assigned in **bank** increments.

Unlike claims 1-6, Wu discloses memory assigned in byte increments. Assignment in byte increments allows one device, i.e., a slow processor to hold up an access request by another device, i.e., a graphics controller to the same bytes in memory, until the slow processor's wait states run out. This causes delays in the opposite device while the slower device completes an access.

In accordance with the principles of the present invention, separate memory **banks** are assigned to the opposite device such that wait state delays of one device do not affect an access to memory by the other device.

Wu fails to disclose, teach, or suggest a first memory portion including a first number of a plurality of memory **banks** and a second memory portion including a second number of a plurality of memory **banks** as claimed by claims 1-6. Therefore, it is respectfully requested that the rejection be withdrawn.

In the Office Action, claims 7-9, 11, 20-21, and 23 appear to be rejected under 35 U.S.C. §102(b) as allegedly being anticipated by Wu. However, the Examiner does not state explicitly the basis for rejecting claims 7-9, 11, 20-21, and 23. Assuming, *arguendo* the Examiner intended to reject claims 7-9, 11, 20-21, and 23 under Wu and in the interest of furthering prosecution, the Applicants respectfully traverse the alleged rejection.

Claims 7-8 now recite, *inter alia*, a plurality of partitions each comprising a number of a plurality of memory **banks**. Claim 11 recites, *inter alia*, a first memory portion including a first number of a plurality of memory **banks** and a second memory portion including a second number of a plurality of memory **banks**. Claims 20-21 recite, *inter alia*, setting a configuration register to partition a shared memory into a first plurality of memory **banks** and a second plurality of memory **banks**. Claim 23 recites, *inter alia*, means for setting a

configuration register to partition a shared memory into a first plurality of memory **banks** and a second plurality of memory **banks**.

The Office Action alleges that Wu discloses partitions which comprise a number of a plurality of memory **banks** (See Office Action, page 3, para. 1-2). The Applicants respectfully disagree.

As discussed above, Wu fails to disclose, teach, or suggest partitions separable between memory **banks** as claimed.

Since Wu fails to disclose, teach, or suggest all limitations of claims 7-8, 11, 20-21, and 23, it is respectfully submitted that claims 7-8, 11, 20-21, and 23 are patentable over the prior art of record. Therefore, it is respectfully requested that the rejection be withdrawn.

Alleged Obviousness of claims 6, 10, and 12 by Wu

In the Office Action, claims 6, 10, and 12 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Wu. The Applicants respectfully traverse the rejection.

Claims 6, 10, and 12 recite, *inter alia*, a first memory portion including a first number of a plurality of memory **banks** and a second memory portion including a second number of a plurality of memory **banks**.

As discussed above, Wu fails to teach or suggest a first memory portion including a first number of a plurality of memory **banks** and a second memory portion including a second number of a plurality of memory **banks** as claimed by claims 6, 10, and 12.

It is therefore respectfully requested that the rejection be withdrawn.

Alleged Anticipation of claims 13-19 by Hughes

In the Office Action, claims 13-19 were rejected under 35 U.S.C. §102(b) as allegedly being anticipated by Hughes, U.S. Patent No. 5,784,582 ("Hughes"). The Applicants respectfully traverse the rejection.

As noted above, the Applicants claim priority from a U.S. Provisional Application filed on November 14, 1997. Since Hughes was issued on July 21, 1998, a priority date of November 14, 1997 renders a rejection under 35 U.S.C. §102(b) improper.

Claims 13-16 now recite, *inter alia*, a second agent to **provide a representation** of a memory access clock signal to access a shared memory in synchronism with access by a first agent. Claims 17-19 now recite, *inter alia*, **providing a representation** of a memory access clock signal in synchronism with the memory access clock signal.

Hughes appears to disclose an arbiter for controlling access to a shared synchronous memory by a processor complex, a refresh unit, an internal bus, and a core bus (See Hughes, col. 4, lines 1-29; Figure 2).

Hughes' processor complex provides a memory clock signal in addition to memory access request information (See Hughes, col. 4, lines 49-58). This memory clock signal is the only clock signal provided to shared memory (See Hughes, col. 4, lines 55-58; Figure 2). Other users of the shared memory (the refresh unit, internal bus, and core bus) provide only memory access request information, i.e., starting address, size, and a direction (See Hughes, col. 5, lines 35-45). The other users of the shared memory do **not** provide any clock signal to shared memory (See Hughes, Figures 2 and 3).

In contrast, claims 13-19 recite, *inter alia*, a second agent to **provide a representation** of a memory access clock signal to access a shared memory in synchronism with access by a first agent. Hence, an agent provides a synchronized representation of a memory access clock signal for its own accesses.

Unlike claims 13-19, Hughes discloses a shared memory which is driven by a single clock signal from a processor complex. The other users of the shared memory do **not** provide any clock signal, much less **provide a representation** of a memory access clock signal. Thus, Hughes fails to disclose, teach, or suggest a second agent to **provide a representation** of a

memory access clock signal to access a shared memory in synchronism with access by a first agent.

It is respectfully submitted that claims 13-19 are patentable over the prior art of record. Therefore, it is respectfully requested that the rejection be withdrawn.

Conclusion

For at least all the above reasons, claims 1-8, and 10-23 are patentable over the prior art of record.

All objections and rejections having been addressed, it is respectfully submitted that the subject application is in condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,
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